CLAIMS

We claim:

1. A unified shader comprising:

an input interface for receiving a packet from a rasterizer;

a shading processing mechanism configured to produce a resultant value from said packet by performing one or more shading operations, wherein said shading operations comprise both texture operations and color operations; and

an output interface configured to send said value to a frame buffer.

2. The shader of claim 1 wherein said input interface receives said packet from said rasterizer using a valid-ready protocol.

3. The shader of claim 1 wherein said output interface sends said value to said frame buffer using a valid-ready protocol.

4. The shader of claim 1 further comprising:

a code partition mechanism to partition code configured to instruct said shading mechanism.

5. The unified shader of claim 4 wherein said partitioning mechanism groups code together by level of indirection.

6. The unified shader of claim 5 further comprises a control logic to process said partitioned code, wherein said control logic comprises:

an input state machine;

a plurality of ALU state machines; and

a plurality of texture machines.

7. The unified shader of claim 1 further comprises:

a register sub-system.

8. The unified shader of claim 1 wherein said shading mechanism further comprises:

a plurality of ALU/memory pairs to perform said shading operations.

9. The unified shader of claim 8 wherein said plurality of ALU/memory pairs constitute a single coherent memory structure, wherein said plurality of ALU/memory pairs are synchronized by a scheduling clock mechanism.

10. The unified shader of claim 9 wherein said plurality of ALU/memory pairs constitute a pipeline for processing said shading operations.

11. The unified shader of claim 9 wherein said wherein said memory structure is a FIFO that does not have an associated buffer.

12. The unified shader of claim 11 wherein said FIFO comprises both data and operation instructions.

13. The unified shader of claim 1 further comprising:

a plurality of additional unified shaders connected to said shader wherein said shader and said additional shaders unified are synchronized by a clock mechanism to process shading operations together.

14. A method for shading comprising:

receiving a packet from a rasterizer;

obtaining a value by performing one or more shading operations, wherein said shading operations comprise both texture operations and color operations; and

sending said value to a frame buffer.

15. The method of claim 14 wherein said receiving uses a valid-ready protocol.

16. The method of claim 14 wherein said sending uses a valid-ready protocol.

17. The method of claim 14 wherein said obtaining comprises:

partitioning a code configured to instruct a unified shader.

18. The method of claim 17 wherein said partitioning groups code together by level of indirection.

19. The method of claim 17 wherein said obtaining further comprises using a control logic to process said partitioned code, wherein said control logic comprises:

an input state machine;

a plurality of ALU state machines; and

a plurality of texture machines.

20. The method of claim 14 wherein said obtaining further comprises using a register sub-system.

21. The method of claim 14 wherein said obtaining comprises:

using a plurality of ALU/memory pairs to perform said shading operations.

22. The method of claim 21 wherein said plurality of ALU/memory pairs constitute a single coherent memory structure, wherein said plurality of ALU/memory pairs are synchronized by a scheduling clock mechanism.

23. The method of claim 22 wherein said plurality of ALU/memory pairs constitute a pipeline for processing said shading operations.

24. The method of claim 22 wherein said memory structure is a FIFO that does not have an associated buffer.

25. The method of claim 24 wherein said FIFO comprises both data and operation instructions.

26. The method of claim 14 wherein said obtaining comprises:

using a plurality of connected unified shaders, wherein said unified shaders are synchronized by a clock mechanism to process said shading operations together.

27. A computer program product comprising:

a computer usable medium having computer readable program code embodied therein configured to shade, said computer program product comprising:

computer readable code configured to cause a computer to receive a packet from a rasterizer;

computer readable code configured to cause a computer to obtain a value by performing one or more shading operations, wherein said shading operations comprise both texture operations and color operations; and

computer readable code configured to cause a computer to send said value to a frame buffer.

28. The computer program product of claim 27 wherein said computer readable code configured to cause a computer to receive uses a valid-ready protocol.

29. The computer program product of claim 27 wherein said computer readable code configured to cause a computer to send uses a valid-ready protocol.

30. The computer program product of claim 27 wherein said computer readable code configured to cause a computer to obtain comprises:

computer readable code configured to cause a computer to partition a code configured to instruct a unified shader.

31. The computer program product of claim 30 wherein said computer readable code configured to cause a computer to partition groups code together by level of indirection.

32. The computer program product of claim 31 wherein said computer readable code configured to cause a computer to obtain further comprises computer readable code configured to cause a computer to use a control logic to process said partitioned code, wherein said control logic comprises:

an input state machine;

a plurality of ALU state machines; and

a plurality of texture machines.

33. The computer program product of claim 32 wherein said computer readable code configured to cause a computer to obtain further comprises computer readable code configured to cause a computer to use a register sub-system.

34. The computer program product of claim 27 wherein said computer readable code configured to cause a computer to obtain comprises:

computer readable code configured to cause a computer to use a plurality of ALU/memory pairs to perform said shading operations.

35. The computer program product of claim 34 wherein said plurality of ALU/memory pairs constitute a single coherent memory structure, wherein said plurality of ALU/memory pairs are synchronized by a scheduling clock mechanism.

36. The computer program product of claim 35 wherein said plurality of ALU/memory pairs constitute a pipeline for processing said shading operations.

37. The computer program product of claim 35 wherein said memory structure is a FIFO that does not have an associated buffer.

38. The computer program product of claim 37 wherein said FIFO comprises both data and operation instructions.

39. The computer program product of claim 27 wherein said computer readable code configured to cause a computer to obtain comprises:

computer readable code configured to cause a computer to use multiple unified shaders wherein said unified shaders are connected.